

IPC-2141A

Design Guide for High-Speed Controlled Impedance Circuit Boards

Developed by the IPC Controlled Impedance Task Group (D-21c) of the High Speed/High Frequency Committee (D-20) of IPC

Supersedes:

IPC-2141 - April 1996

Users of this publication are encouraged to participate in the development of future revisions.

Contact:

IPC 2215 Sanders Road Northbrook, Illinois 60062-6135 Tel 847 509.9700 Fax 847 509.9798

Table of Contents

	SCOPE		4.3.2	Even Mode, Odd Mode, Common Mode, and Differential Mode Impedances	21
2	APPLICABLE DOCUMENTS		4.4	Balanced Line Equations	
2.1	IPC	1	4.4.1	Edge-Coupled Surface Microstrip	
3 E	ENGINEERING DESIGN OVERVIEW	1	4.4.2	Edge-Coupled Symmetric Stripline	23
3.1	Device Selection	2	4.4.3	Broadside-Coupled Symmetric Stripline	23
3.2	Interconnection	2	4.5	Controlled Impedance Design Rules	23
3.2.1	Connectors	2	4.5.1	Effect of External and Device Impedance	23
3.2.2	Cables	3	4.5.2	Material Properties and Transmission	
3.3	Printed Board and Printed Board Assemblies .	3		Line Geometry	
3.3.1	Board Design	3	4.5.3	High Impedance	
3.4	Performance Requirements	4	4.5.4	Impedance Design Considerations	23
3.4.1	Power Distribution System	4	4.5.5	Secondary Controlled Impedance Design Factors	23
3.4.2	Relative Permittivity	5	4.6	Crosstalk Guidelines	
3.4.3	Measuring Effective Relative Permittivity	6	4.6.1	Crosstalk Implementation	
3.4.4	Loss tangent (tanδ, or dissipation factor)	6	4.0.1	Design Guidelines for Controlled	4
3.4.5	Bandwidth	6	4.7	Impedance Test Structures	24
3.4.6	Capacitive Line Versus Transmission		4.7.1	Purpose of Test Coupon	
	Line Environment		4.7.2	Test Interconnect Placement	
3.4.7	Propagation in a Transmission Line		4.7.3	Test Interconnect Geometry	25
3.4.8	Critical Signal Speed		4.7.4	Test Interconnect Routing	
3.4.9	Critical Line Length		4.7.5	Nomenclature	
3.4.10	1 0		4.7.6	Additional Guidelines for Testing	
3.4.11	Signal Loading Effects	. 12		Panel Coupons	27
3.4.12			4.8	Decoupling/Capacitor Guidelines	27
3.4.13	Termination of Nets	. 12	4.8.1	Decoupling Capacitance	27
3.4.14	Additional Signal Integrity Issues	. 14	4.8.2	Capacitor Model	28
3.4.15	Noise	. 14	4.8.3	Decoupling/Capacitor Design Rules	28
	DESIGN OF CONTROLLED		4.9	EMI Considerations in Design Layout	28
I	MPEDANCE CIRCUITS	. 15	4.9.1	Reasons for Considering EMI in	
4.1	Unbalanced Line Configurations	. 16		Design Layout	28
4.1.1	Microstrip	. 16	4.9.2	Pulse Transition Rates and Times	28
4.1.2	Stripline	. 16	4.9.3	Suggested EMI Layout Practices	28
4.2	Unbalanced Line Equations	. 17	5 D	ESIGN FOR MANUFACTURING	30
4.2.1	Capacitance per Unit Length	. 18	5.1	Process Rules in CAD	30
4.2.2	Surface Microstrip, Figure 4-3(a)	. 18	5.2	Design Complexity and Correlation to Cost	31
4.2.3	Embedded Microstrip, Figure 4-3(b)	. 18	6 B		
4.2.4	Symmetric Stripline, Figure 4-3(c)	. 18		PATA DESCRIPTION	
4.2.5	Asymmetric Stripline, Figure 4-3(d)	. 19	6.1	Details of Construction	
4.2.6	Wire Stripline, Figure 4-3(e)	. 19	6.1.1	Controlled Construction	31
4.2.7	Wire Microstrip, Figure 4-3(f)	. 19	6.1.2	Controlled Performance - Controlled Capacitance or Controlled Impedance	31
4.3	Balanced Line Configuration		6.2	Isolation of Data by Net Class (Noise,	
4.3.1	Even Versus Odd Mode Propagation	. 20		Timing, Capacitance, and Impedance)	31

6.3	Electrical Performance	32	9.3.3	Con	nectors	43
7 M	ATERIALS	32	9.3.4	Prob	es	43
7.1	Resin Systems		9.3.5	Test	Fixtures	44
7.2	Reinforcements		9.4	TDR	Operation	. 44
7.3	Prepregs, Bonding Layers and Adhesives		9.4.1	Oper	rating Procedures	44
7.4	Frequency Dependence		9.4.2	Test	Considerations	44
			9.4.3	Oper	rator Requirements	44
	ABRICATION		9.4.4		Example, Unbalanced	
8.1	General			Tran	smission Line	45
8.1.1	Data		9.4.5		Example, Balanced smission Line	15
8.1.2	Pattern Generation and Transfer		0.4.6			
8.1.3	Machined Features		9.4.6		/Fail Testing	
8.2	Preproduction Processes		9.4.7		Information	
8.2.1	Artwork Verification	33	9.5		Structure	
8.2.2	Panelization	33	9.5.1		dard Test Coupon	
8.2.3	Tooling	33	9.6		Calibration	
8.2.4	Photoplotting	33	9.6.1		oration Artifacts	
8.2.5	Artwork Inspection	33	9.7	Alte	rnative TDR Design	47
8.3	Production Processes	34				
8.3.1	Processing Considerations	34			Figure	
8.3.2	Laminate, Expose & Develop Cores	34			Figures	
8.3.3	Innerlayer Etching	34	Figure 3	3-1	Relative permittivity of FR4 as a function of	
8.3.4	Scan (AOI)	34			frequency for different glass reinforcement	
8.3.5	Lamination	36			and percent resin content. The data used to generate these curves has been provided by	
8.3.6	Numerically Controlled (NC) Equipment	36			Park/Nelco.	
8.3.7	Hole Formation	36	Figure 3	3-2	Step-like Waveforms. Transition duration	_
8.3.8	Routing (NC Profile)	36			values are shown in parenthesis	8
8.3.9	Dimensional Inspection	36	Figure 3	3-3	Spectra of the derivatives of the waveforms shown in Figure 3-2.	8
8.3.10	Electrolytic (Pattern) Plate	36	Figure 3	3-4	Termination of Nets.	
8.3.11	Outer Layer Strip, and/or Etch		Figure 4	1-1	Diagrams of two types of unbalanced	
8.3.12	• •				transmission line configurations	. 16
8.4	Impact of Defects at High Frequencies		Figure 4	1-2	Circuit schematic showing unbalanced transmission line	17
8.4.1	Copper		Figure 4	1_3	Typical unbalanced line configurations	
8.4.2	Substrate		Figure 4		Balanced line structure.	
8.5	Data Description		Figure 4		Circuit schematic showing balanced	. 20
8.5.1	Type of CAD Data		i igui o	. 0	transmission line.	. 20
8.5.2	Customer Interface		Figure 4	1-6	Cross-sections of typical balanced line configuration.	21
9 TI	IME DOMAIN REFLECTOMETRY TESTING	38	Figure 4	1-7	Electric field lines for even (top) and odd	. ∠ 1
9.1	Description of Time-Domain Reflectometry .		J		(bottom) modes of propagation in a balanced transmission line. The two smaller black	
9.1.1	Mathematics of TDR Waveform				rectangles in each sketch represent the two	
9.2	Uses of TDR				signal lines and the long black rectangle	20
9.2.1	Computation of Characteristic Impedance		Figure /	1_Ω	represents the reference plane	. 22
9.2.2	Comparison to Other Methods		Figure 4	+-0	Impedance test interconnect contact pad geometry and drilled hole size. All dimensions	S
9.3	TDR System Description				are reference.	
9.3.1	System Components and Their Requirements		Figure 4	1-9	Impedance coupon design. All dimensions	27
9.3.1	Cables		Figure 6	2_1	are reference.	
7.3.4	Caules	43	Figure 8	ו -ר	Flow Chart of Preproduction Processes	. ა4

IPC-2141A March 2004

Figure 8-2 Figure 9-1	Production Process Flow Chart	Figure 9-4	reflected pulses. The reflected and incident	
Figure 9-2	Pulse generated and sampled by TDR unit. This is the pulse that is launched onto the TDR output connector. The arrow in the figure on the left depicts the direction of propagation of the pulse, assuming the TDR unit is to the left. The arrow in the figure on the right shows the time axis of the recorded TDR waveform		pulses add. Because the incident pulse is a step, the reflected positive reflected pulse appears to sit on top of the high state of the incident pulse	
		Figure 9-5	TDR waveform of a positive reflection 4	
		Figure 9-6	Depiction of coupon connection for unbalanced transmission line 49	
		Figure 9-7	TDR testing of differential lines 40	
Figure 9-3	Pulse reflected from an impedance dis- continuity and traveling back toward the TDR unit. The arrow indicates the direction	Figure 9-8	Sketch of layout of alternative TDR system 4	
	of propagation (compare Figure 9-2, left side). The reflected pulse is positive in this example		Tables	
	because the reflection coefficient at the impedance discontinuity is greater than 0 39	Table 3-1	Typical Data for Some Logic Families (critical line length is described in 3.4.9)	

March 2004 IPC-2141A

Design Guide for High-Speed Controlled Impedance Circuit Boards

1 SCOPE

This guide is intended to be used by circuit designers, packaging engineers, printed board fabricators, and procurement personnel so that all may have a common understanding of each other's area.

The goal in packaging is to transfer a signal from one device to one or more other devices, through a conductor. High-speed designs are defined as designs in which the interconnecting properties affect circuit performance and require unique consideration.

The term "high-speed" as applied to logic or digital designs needs clarification in its usage. The three most common interpretations of high-speed are as follows. (1) High-speed as a reference to the rate of change of signal amplitude with time (frequently called the edge rate of a pulse) constitutes the most important usage. The edge rate puts the greatest performance demand on interconnecting structures. (2) High-speed as a reference to the data transmission rate (bits or bytes per second) is often used to describe the "speed" of a system. However, high data rates can be achieved with parallel bus architectures that do not necessarily require improved performance of an interconnecting structure. (3) High-speed as a reference to the speed (distance per unit time) of a signal propagating between devices has the smallest usage and, in many cases, is not important to the application.

Controlled impedance is the maintenance of some specified tolerance in the characteristic impedance of an interconnect line (transmission line) that is used to connect different devices on a circuit. Controlled impedance is often a design consideration for high-speed digital or high-frequency analog circuits. However, the reverse is not true, that is, high-speed digital or high-frequency analog circuit designs may not need to consider controlled impedance. The purpose of this document is to help the designer understand when controlled impedance should be considered in his/her circuit design and to describe concepts important to controlled impedance design.

2 APPLICABLE DOCUMENTS

The following standards contain provisions which, through reference in this text, constitute provisions of this document. At the time of publication, the editions indicated were valid. All standards are subject to revision, and parties to agreements based on this standard are encouraged to investigate the possibility of applying the most recent editions of the standards listed below.

2.1 IPC1

IPC T-50 Terms and Definitions for Interconnecting and Packaging Electronic Circuits

IPC-D-356 Bare Substrate Electrical Test Data Format

IPC-TM-650 Test Methods Manual²

2.5.5.7 11/92 Characteristic Impedance of Lines on Printed Boards by TDR

IPC-2220 Design Standard Series

IPC-2251 Design Guidelines for the Packaging of High Speed Electronic Circuits

IPC-2252 Design and Manufacture Guide for RF/Microwave Circuit Boards

IPC-4101 Specification for Base Materials for Rigid and Multilayer Printed Boards

IPC-4103 Specification for Base Materials for High Speed/High Frequency Applications

References, if presented at the end of a section, provide a more comprehensive treatment of the subject of that section.

3 ENGINEERING DESIGN OVERVIEW

Packaging of electronic equipment has traditionally been an area for mechanical considerations. However, today's packaging designs are becoming more complex because of the faster switching speeds and higher input/output densities available from today's electronic technologies. To take maximum advantage of device density and speed, designers must pay much more attention to problems of electromagnetic wave propagation phenomena associated with transmission of high-speed pulsed/switched signals within the system. New design disciplines and design strategies are needed. Controlled impedance circuit boards are a part of this strategy.

Interconnection and the packaging of electronic components primarily has been the domain of mechanical designers who were concerned with such factors as weight, volume, power, and form factor, and when interconnections

^{1.} www.ipc.org

^{2.} Current and revised IPC Test Methods are available through IPC-TM-650 subscription and on the IPC Web site (www.ipc.org/html/testmethods.htm).