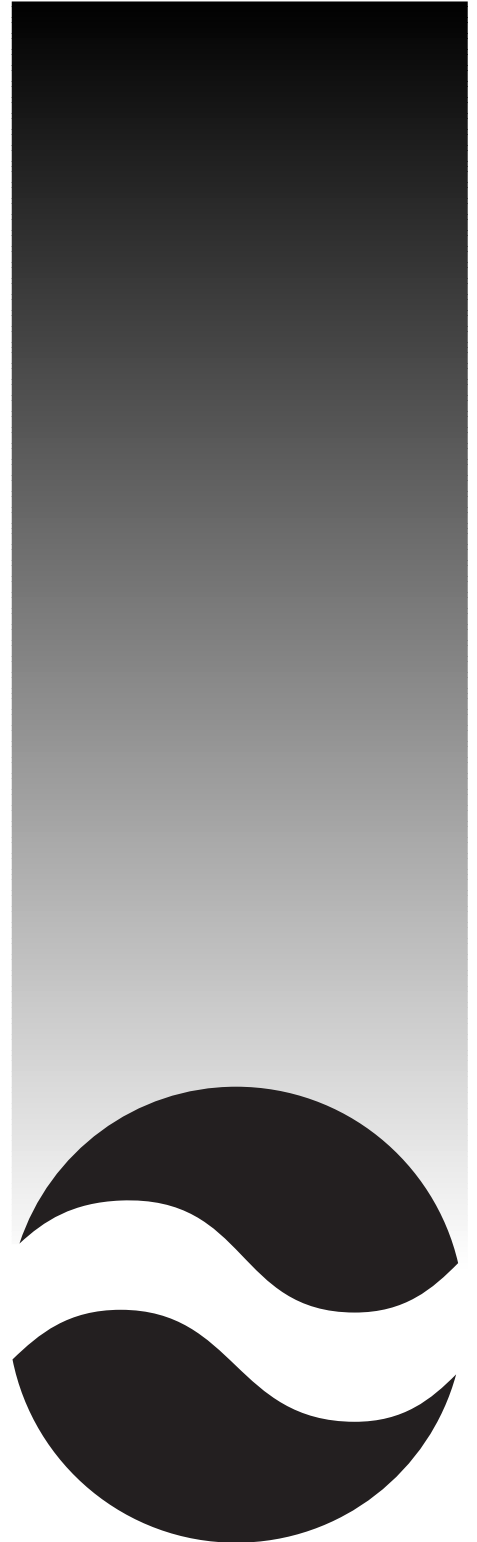


IPC/EIA J-STD-028
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JOINT INDUSTRY STANDARD

Performance
Standard for
Construction of
Flip Chip and
Chip Scale Bumps





ASSOCIATION CONNECTING
ELECTRONICS INDUSTRIES



IPC/EIA J-STD-028

Performance Standard for Construction of Flip Chip and Chip Scale Bumps

About This Document

This document is intended to report on the work being done by several organizations concerned with the design of bare die in flip chip or chip scale configurations. Details were developed by companies who have implemented the processes described herein and have agreed to share their experiences. Readers are encouraged to communicate to the appropriate trade associations or societies any comments or observations regarding details published in this document, or ideas for additional details that would serve the industry.

Users of this standard are encouraged to participate in the development of future revisions.

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Performance Standard for Construction of Flip Chip and Chip Scale Bumps

1 SCOPE

This standard establishes the construction detail requirements for bumps and other terminal structures on flip chips and chip scale carriers. All flip chip and chip scale device terminals shall meet the designated standards detailed in this document which includes such diverse terminations as solder bumps, columns, non-melting stand-offs and conductive polymer deposits. The specific standards for different terminations will therefore be appropriately matched to the particular interconnection.

1.1 Purpose The purpose of this document is to establish a set of designations and expectations for product performance for the manufacturer and user of flip chip or chip scale devices. Included in this will be the flexibility to implement the best commercial practices and evolving improvements on those practices.

1.2 Intent The intent is to recognize a large variety of terminal structures for a wide range of applications ranging from highest reliability computer, space and military applications to disposable commodity applications. Subsections in this document will provide for the flexibility to meet the cost and performance requirements.

1.3 Presentation All dimensions and tolerances in this standard are expressed in metric units with millimeters being the main form of dimensional expression. Inches may be shown in brackets as appropriate and are not always a direct conversion depending on the round-off or the required precision. Users are cautioned to employ a single dimensioning system, and not intermix millimeters and inches. Reference information is shown in parentheses ().

1.4 Interpretation **Shall**, the emphatic form of the verb, is used throughout this standard whenever a requirement is intended to express a provision that is mandatory. Deviation from a **shall** requirement may be considered if sufficient data is supplied to justify the exception.

The words *should* and *may* are used whenever it is necessary to express non-mandatory provision.

Will, is used to express a declaration of purpose.

To assist the reader, the word **shall** is presented in bold characters.

1.5 Organization of Design Information This standard is organized into various sections in order to provide information for the design of flip chip devices. The main sections with their points of emphasis are:

Section 3 Design Considerations

Section 4 Quality Assessments

1.6 Order of Precedence In the event of any conflict in the development of new designs, the following order or precedence should prevail:

1. The customer requirements.
2. Substrate design rules.
3. Bump design rules.
4. This standard.

2 APPLICABLE DOCUMENTS

The following documents contain provisions which, through reference in this text, constitute a part of the J-STD-028. At the time of publication, the editions indicated were valid. All documents are subject to revision and parties to agreements based on this standard are encouraged to investigate the possibility of applying the most recent editions.