

IPC-7095B

Design and Assembly Process Implementation for BGAs

Developed by the Device Manufacturers Interface Committee of IPC



Supersedes:

IPC-7095A - October 2004 IPC-7095 - August 2000 Users of this publication are encouraged to participate in the development of future revisions.

Contact:

IPC 3000 Lakeside Drive, Suite 309S Bannockburn, Illinois 60015-1249 Tel 847 615.7100 Fax 847 615.7105

Table of Contents

1 5	SCOPE	1	4.3.1	Industry Standards for BGA	16
1.1	Purpose	1	4.3.2	Ball Pitch	17
1.2	Intent	1	4.3.3	BGA Package Outline	18
2 <i>A</i>	APPLICABLE DOCUMENTS	1	4.3.4	Ball Size Relationships	19
2.1	IPC		4.3.5	Coplanarity	19
2.2	JEDEC		4.4	Component Packaging Style Considerations	19
		1	4.4.1	Solder Ball Alloy	20
	SELECTION CRITERIA AND MANAGING SGA IMPLEMENTATION	2	4.4.2	Ball Attach Process	20
3.1	Description of Infrastructure		4.4.3	Ceramic Ball Grid Array	21
3.1.1	Land Patterns and Circuit Board		4.4.4	Ceramic Column Grid Arrays	21
5.1.1	Considerations	3	4.4.5	Tape Ball Grid Arrays	22
3.1.2	Technology Comparison	5	4.4.6	Multiple Die Packaging	22
3.1.3	Assembly Equipment Impact	7	4.4.7	System-in-Package (SiP)	23
3.1.4	Stencil Requirements	7	4.4.8	3D Folded Package Technology	23
3.1.5	Inspection Requirements	8	4.4.9	Ball Stack, Package-on-Package	23
3.1.6	Test	8	4.4.10	Folded and Stacked Packaging Combination .	24
3.2	Time-to-Market Readiness	8	4.4.11	Benefits of Multiple Die Packaging	24
3.3	Methodology	9	4.5	BGA Connectors	24
3.4	Process Step Analysis	9	4.5.1	Material Considerations for BGA Connectors	24
3.5	BGA Limitations and Issues	9	4.5.2	Attachment Considerations for	
3.5.1	Visual Inspection	9		BGA Connectors	
3.5.2	Moisture Sensitivity	9	4.6	BGA Construction Materials	
3.5.3	Thermally Unbalanced BGA Design	10	4.6.1	Types of Substrate Materials	
3.5.4	Rework	10	4.6.2	Properties of Substrate Materials	
3.5.5	Cost	11	4.7	BGA Package Design Considerations	
3.5.6	Availability	12	4.7.1	Power and Ground Planes	
3.5.7	Voids in BGA	12	4.7.2	Signal Integrity	28
3.5.8	Standardization Issues	12	4.7.3	Heat Spreader Incorporation Inside the Package	28
3.5.9	Reliability Concerns	12	4.8	BGA Package Acceptance Criteria and	20
4 (COMPONENT CONSIDERATIONS	12	7.0	Shipping Format	28
4.1	Component Packaging Comparisons	12	4.8.1	Missing Balls	28
	and Drivers	12	4.8.2	Voids in Solder Balls	
4.1.1	Package Feature Comparisons	12	4.8.3	Solder Ball Attach Integrity	29
4.1.2	BGA Package Drivers	13	4.8.4	Package Coplanarity	
4.1.3	Cost Issues	13	4.8.5	Moisture Sensitivity (Baking, Storage,	
4.1.4	Component Handling	13		Handling, Rebaking)	30
4.1.5	Thermal Performance	13	4.8.6	Shipping Medium (Tape and Reel,	
4.1.6	Real Estate	13		Trays, Tubes)	
4.1.7	Electrical Performance	14	4.8.7	Solder Ball Alloy	31
4.2	Die Mounting in the BGA Package	14	5 P	CBS AND OTHER MOUNTING STRUCTURES	31
4.2.1	Wire Bond		5.1	Types of Mounting Structures	31
4.2.2	Flip Chip	15	5.1.1	Organic Resin Systems	
4.3	Standardization		5.1.2	Inorganic Structures	

5.1.3	Layering (Multilayer, Sequential	6.4	Impact of Wave Solder on Top Side BGAs	57
	or Build-Up)	6.4.1	Top Side Reflow	57
5.2	Properties of Mounting Structures	6.4.2	Impact of Top Side Reflow	57
5.2.1	Resin Systems	6.4.3	Methods of Avoiding Top Side Reflow	58
5.2.2	Reinforcements	6.4.4	Top Side Reflow for Lead-Free Boards	59
5.2.3	Laminate Material Properties	6.5	Testability and Test Point Access	59
5.2.4	Reliability Concerns with High Lead-Free Soldering Temperatures	6.5.1	Component Testing	59
5.2.5	Thermal Expansion	6.5.2	Damage to the Solder Balls During Test	60
5.2.6	Glass Transition Temperature	6.5.3	and Burn-In	
5.2.7	Moisture Absorption	6.5.4	Assembly Testing	
5.3	Surface Finishes	6.6	Other Design for Manufacturability Issues	
5.3.1	Hot Air Solder Leveling (HASL)	6.6.1	Panel/Subpanel Design	
5.3.2	Organic Surface Protection (Organic Solderability Preservative) OSP Coatings 37	6.6.2	In-Process/End Product Test Coupons	
5.3.3	Noble Platings/Coatings	6.7	Thermal Management	65
5.4	Solder Mask	6.7.1	Conduction	65
5.4.1	Wet and Dry Film Solder Masks	6.7.2	Radiation	66
5.4.2	Photoimageable Solder Masks	6.7.3	Convection	67
5.4.3	Registration	6.7.4	Thermal Interface Materials	67
5.4.4	Via Protection	6.7.5	Heat Sink Attachment Methods for BGAs	67
5.5	Thermal Spreader Structure Incorporation	6.8	Documentation and Electronic Data Transfer	69
5.5	(e.g., Metal Core Boards)	6.8.1	Drawing Requirements	
5.5.1	Lamination Sequences	6.8.2	Equipment Messaging Protocols	
5.5.2	Heat Transfer Pathway	6.8.3	Specifications	71
	RINTED CIRCUIT ASSEMBLY DESIGN CONSIDERATION		SSEMBLY OF BGAS ON PRINTED	71
6.1	Component Placement and Clearances	7.1	SMT Assembly Processes	71
6.1.1	Pick and Place Requirements	7.1.1	Solder Paste and Its Application	71
6.1.2	Repair/Rework Requirements	7.1.2	Component Placement Impact	73
6.1.3	Global Placement	7.1.3	Vision Systems for Placement	73
6.1.4	Alignment Legends (Silkscreen, Copper	7.1.4	Reflow Soldering and Profiling	74
	Features, Pin 1 Identifier)	7.1.5	Material Issues	78
6.2	Attachment Sites (Land Patterns and Vias) 48	7.1.6	Vapor Phase	78
6.2.1	Big vs. Small Land and Impact on Routing 48	7.1.7	Cleaning vs. No-Clean	79
6.2.2	Solder Mask vs. Metal Defined Land Design 48	7.1.8	Package Standoff	79
6.2.3	Conductor Width	7.2	Post-SMT Processes	80
6.2.4	Via Size and Location 50	7.2.1	Conformal Coatings	80
6.3	Escape and Conductor Routing Strategies 51	7.2.2	Use of Underfills and Adhesives	81
6.3.1	Escape Strategies	7.2.3	Depaneling of Boards and Modules	84
6.3.2	Surface Conductor Details	7.3	Inspection Techniques	84
6.3.3	Dog Bone Through Via Details 54	7.3.1	X-Ray Usage	84
6.3.4	Design for Mechanical Strain	7.3.2	X-Ray Image Acquisition	85
6.3.5	Uncapped Via-in-Pad and Impact on Reliability Issues	7.3.3	Definition and Discussion of X-Ray System Terminology	86
6.3.6	Fine Pitch BGA Microvia in Pad Strategies 56	7.3.4	Analysis of the X-Ray Image	
	The Then Berrymerovia in Tag Strategies 30			

7.3.6 7.3.7	BGA Standoff Measurement Optical Inspection		8.5.4	Reliability of Solder Attachments of Ceramic Grid Array	. 121
7.3.8	Destructive Analysis Methods		8.5.5	Lead-Free Soldering of BGAs	. 121
7.4	Testing and Product Verification		8.6	Design for Reliability (DfR) Process	. 127
7.4.1	Electrical Testing		8.7	Validation and Qualification Tests	. 128
7.4.2	Test Coverage		8.8	Screening Procedures	. 128
7.4.3	Burn-In Testing		8.8.1	Solder Joint Defects	. 128
7.4.4	Product Screening Tests		8.8.2	Screening Recommendations	. 128
7.5	Assembly Process Control Criteria for Plastic BGAs			EFECT AND FAILURE ANALYSIS ASE STUDIES	. 129
7.5.1	Voids	95	9.1	Solder Mask Defined BGA Conditions	. 129
7.5.2	Solder Bridging	. 106	9.1.1	Solder Mask Defined and Nondefined Lands .	. 129
7.5.3	Opens	. 106	9.1.2	Solder Mask Defined Land on	
7.5.4	Cold Solder	. 106		Product Board	
7.5.5	Defect Correlation/Process Improvement	. 106	9.1.3	Solder Mask Defined BGA Failures	
7.5.6	Insufficient/Uneven Heating	. 107	9.2	Over-Collapse BGA Solder Ball Conditions	. 130
7.5.7	Component Defects	. 107	9.2.1	BGA Ball Shape without Heat Slug 500 µm Standoff Height	. 130
7.6	Repair Processes	. 108	9.2.2	BGA Ball Shape with Heat Slug 375 μm	
7.6.1	Rework/Repair Philosophy	. 108		Standoff Height	. 130
7.6.2	Removal of BGA	. 108	9.2.3	BGA Ball Shape with Heat Slug 300 μm	
7.6.3	Replacement	. 109	0.2.4	Standoff Height	
8 RE	ELIABILITY	. 111	9.2.4	Critical Solder Paste Conditions	
8.1	Accelerated Reliability Testing	. 111	9.2.5	Thicker Paste Deposit	. 131
8.2	Damage Mechanisms and Failure of		9.2.6	Void Determination Through X-Ray and Cross-Section	. 131
0.0.1	Solder Attachments	. 112	9.2.7	Voids and Uneven Solder Balls	. 132
8.2.1	Comparison of Thermal Fatigue Crack Growth Mechanism in SAC vs. Tin/		9.2.8	Eggshell Void	. 132
	Lead BGA Solder Joints	. 113	9.3	BGA Interposer Bow and Twist	. 132
8.2.2	Mixed Alloy Soldering	. 113	9.3.1	BGA Interposer Warp	. 133
8.3	Solder Joints and Attachment Types	. 115	9.3.2	Solder Joint Opens Due to Interposer Warp	. 133
8.3.1	Global Expansion Mismatch	. 116	9.4	Solder Joint Conditions	. 133
8.3.2	Local Expansion Mismatch	. 116	9.4.1	Target Solder Condition	. 134
8.3.3	Internal Expansion Mismatch		9.4.2	Solder Balls With Excessive Oxide	. 134
8.4	Solder Attachment Failure		9.4.3	Evidence of Dewetting	
8.4.1	Solder Attachment Failure Classification	. 116	9.4.4	Mottled Condition	
8.4.2	Failure Signature-1: Cold Solder	. 117	9.4.5	Tin/lead Solder Ball Evaluation	
8.4.3	Failure Signature-2: Land, Nonsolderable		9.4.6	SAC Alloy	
8.4.4	Failure Signature-3: Ball Drop		9.4.7	Cold Solder Joint	. 135
8.4.5	Failure Signature-4: Missing Ball		9.4.8	Incomplete Joining Due to Land	125
8.4.6	Failure Signature-5: Package Warpage		0.40	Contamination	
8.4.7	Failure Signature-6: Mechanical Failure		9.4.9	Deformed Solder Ball Contamination	
8.4.8	Failure Signature 7: Insufficient Reflow		9.4.10	Deformed Solder Ball	. 136
8.5	Critical Factors to Impact Reliability		9.4.11	Insufficient Solder and Flux for Proper Joint Formation	. 136
8.5.1	Package Technology	. 119	9.4.12	Reduced Termination Contact Area	. 136
8.5.2	Stand-off Height	. 120	9.4.13	Excessive Solder Bridging	. 137
8.5.3	PCB Design Considerations	. 121	9.4.14	Incomplete Solder Reflow	. 137

9.4.15	Disturbed Solder Joint	137	Figure 4-18	BGA connector	25
9.4.16	Missing Solder	137	Figure 4-19	Example of missing balls on a BGA component	28
	GLOSSARY AND ACRONYMS		Figure 4-20	Example of voids in eutectic solder balls at incoming inspection	29
11 E	BIBLIOGRAPHY AND REFERENCES	139	Figure 4-21	Examples of solder ball/land surface conditions	29
	Figures		Figure 4-22	Establishing BGA coplanarity requirement 3	30
Figure 3	BGA package manufacturing process	2	Figure 4-23	Ball contact positional tolerance	30
Figure 3			Figure 5-1	Examples of different build-up constructions . 3	32
Figure 3	· · ·		Figure 5-2	Expansion rate above T _g	34
Figure 3			Figure 5-3	Hot air solder level (HASL) surface topology	
Figure 3				comparison	36
Figure 3			Figure 5-4	Black pad related fracture showing crack between Nickel & Ni-Sn intermetallic layer	30
Figure 3			Eiguro 5 5	· ·	50
Figure 3	3-8 BGA warpage		Figure 5-5	Crack location for a) black pad related failure and (b) interfacial fracture when using ENIG surface finish	38
Figure 4	ground for the die. The rest of the area has been used for signal routing but has been		Figure 5-6	Typical mud crack appearance of black pad Surface	
Figure 4	covered with solder mask to isolate it from the conductive adhesive under the die	14	Figure 5-7	A large region of severe black pad with corrosion spikes protruding into nickel rich layer through phosphorus rich layer underneath immersion gold surface	39
	fill and squeeze-out. The picture on the top shows the adhesive dispense pattern on the die site. The picture on the bottom shows		Figure 5-8	Graphic depiction of electroless nickel, electroless palladium/immersion gold	40
	the placed glass die to view voids and filling characteristics. The adhesive provides full die		Figure 5-9	Graphic depiction of directed immersion gold	40
	coverage for attachment but partial coverage		Figure 5-10	Work and turn panel layout	43
	to ground through a smaller than die ground pad, allowing a larger portion of the area		Figure 5-11	Distance from tented land clearance	43
	under the die for signal routing saving		Figure 5-12	Via plug methods	45
	valuable real estate and making the resulting package smaller	15	Figure 5-13	Solder filled and tented via blow-out	46
Figure 4			Figure 5-14	Metal core board construction examples	46
Figure 4			Figure 6-1	BGA alignment marks	47
Figure 4			Figure 6-2	Solder lands for BGA components	49
Figure 4			Figure 6-3	Metal defined land attachment profile	49
Figure 4		21	Figure 6-4	Solder mask stress concentration	49
i iguic -	(CBGA) package	21	Figure 6-5	Solder joint geometry contrast	49
Figure 4	1-8 Ceramic ball grid array (CBGA) package	21	Figure 6-6	Good/bad solder mask design	50
Figure 4			Figure 6-7	Examples of metal-defined land	50
	array (CCGA) package	21	Figure 6-8	Quadrant dog bone BGA pattern	51
Figure 4	I-10 Polyimide film based lead-bond μBGA package substrate furnishes close coupling between die pad and ball contact		Figure 6-9	Square array	52
		22	Figure 6-10	Rectangular array	52
Figure 4	4-11 Comparing in-package circuit routing capability of the single metal layer tape		Figure 6-11	Depopulated array	52
J			Figure 6-12	Square array with missing balls	52
	substrate to two metal layer tape substrate		Figure 6-13	Interspersed array	53
Figure 4		23	Figure 6-14	Conductor routing strategy	53
Figure 4	SiP assembly		Figure 6-15	BGA dogbone land pattern preferred direction for conductor routing	55
Figure 4	· · · · · · · · · · · · · · · · · · ·		Figure 6-16	Preferred screw and support placement	
Figure 4			Figure 6-17	Connector screw support placement	
Figure 4 Figure 4	· · · · · · · · · · · · · · · · · · ·	24	Figure 6-18	Cross section of 0.75 mm ball with via-in- pad structure (Indent to the upper left of	
5	BGA package	24		the ball is anartifact.)	55

Figure 6-19	Cross section of via-in-pad design showing via cap and solder ball		Figure 7-12	Examples of underfill voids - small, medium and large; upper left, lower left and left of solder balls, respectively	32
Figure 6-20	Via-in-pad process descriptions		Figure 7-13	Example of partial underfill - package was	
Figure 6-21	Microvia example		1 19410 7 10	pulled from the PCB and dark underfill can	
Figure 6-22	Microvia in pad voiding			be seen in the corners 8	2
Figure 6-23	Ground or power BGA connection		Figure 7-14	Corner applied adhesive 8	3
Figure 6-24 Figure 6-25	Example of top side reflow joints Example of wave solder temperature profile		Figure 7-15	Critical dimension for application of prereflow corner glue	3
Figure 6-26	of top-aide of mixed component assembly Heat pathways to BGA solder joint during wave soldering		Figure 7-16	Typical corner glue failure mode in shock if glue area is too low - Solder mask rips off board and does not protect the solder	
Figure 6-27	Methods of avoiding BGA topside solder	. 50		joints 8	3
rigule 0-27	joint reflow	59	Figure 7-17	Fundamentals of X-ray technology 8	5
Figure 6-28	An example of a side contact made with a		Figure 7-18	X-ray example of missing solder balls 8	5
Figure 6-29	tweezers type contact	60	Figure 7-19	X-ray example of voiding in solder ball contacts	
	on the bottom of a solder ball	60	Figure 7-20	Manual X-ray system image quality 8	
Figure 6-30	Area array land pattern testing	62	Figure 7-21	Example of X-ray pin cushion distortion	Ĭ
Figure 6-31	Board panelization	65	riguio 7 21	and voltage blooming8	6
Figure 6-32	Comb pattern examples	66	Figure 7-22	Transmission image (2D) 8	6
Figure 6-33	Heat sink attached to a BGA with		Figure 7-23	Tomosynthesis image (3D) 8	
	an adhesive	68	Figure 7-24	Laminographic cross-section image (3D) 8	
Figure 6-34	Heat sink attached to a BGA with a clip that hooks onto the component substrate	68	Figure 7-25	Transmission example 8	
Figure 6-35	Heat sink attached to a BGA with a clip	. 00	Figure 7-26	Oblique viewing board tilt 8	
riguic 0 00	that hooks into a through-hole on the		Figure 7-27	Oblique viewing detector tilt 8	
	printed circuit board	68	Figure 7-28	Top down view of FBGA solder joints 8	
Figure 6-36	Heat sink attached to a BGA with a clip that		Figure 7-29	Oblique view of FBGA solder joints	
	hooks onto a stake soldered in the printed circuit board	69	Figure 7-30	Tomosynthesis	
Figure 6-37	Heat sink attached to a BGA by wave		•		
	soldering its pins in a through-hole in		Figure 7-31	Scanned beam X-ray laminography 8	
	the printed circuit board	69	Figure 7-32	Scanning acoustic microscopy	
Figure 7-1	Aspect and area ratios for complete paste release	72	Figure 7-33	Endoscope example	-1
Figure 7-2	High lead and eutectic solder ball and joint comparison		Figure 7-34	Lead-free 1.27 mm pitch BGA reflowed in nitrogen and washed between SMT passes)1
Figure 7-3	Example of peak reflow temperatures at various locations at or near a BGA		Figure 7-35	Lead-free BGA reflowed in air and washed between SMT passes	12
Figure 7-4	Schematic of reflow profile for tin/lead		Figure 7-36	Engineering crack evaluation technique 9	3
Figure 7-5	An example of tin/lead profile with multiple	75	Figure 7-37	A solder ball cross sectioned through a void in the solder ball	3
Figure 7-6	thermocouples		Figure 7-38	Cross-section of a crack initiation at the ball/pad interface	3
	assemblies	76	Figure 7-39	No dye penetration under the ball 9	14
Figure 7-7	Examples of lead-free profiles with soak (top) and ramp to peak (bottom) with multiple thermocouples. The profiles		Figure 7-40	Corner balls have 80-100% dye penetration which indicate a crack	4
Figure 7-8	with soak tend to reduce voids in BGAs Locations of thermocouples on a board	76	Figure 7-41	Small voids clustered in mass at the ball-to-land interface	6
Figure 7-9	with large and small components	77	Figure 7-42	X-ray image of solder balls with voids at 50 kV (a) and 60 kV (b)9	7
J	on a BGA	77	Figure 7-43	Typical size and location of various types of voids in a BGA solder joint	8(
Figure 7-10	Effect of having solder mask relief around the BGA lands of the board	80	Figure 7-44	Example of voided area at land and board Interface	
Figure 7-11	Flow of underfill between two parallel surfaces	82	Figure 7-45	Typical flow diagram for void assessment 10	

Figure 7-46	Voids in BGAs with crack started at corner lead 1	04	Figure 8-21	Micrograph of a cross-section of a BGA SnAgCu solder ball, assembled onto a board
Figure 7-47	Examples of suggested void protocols 1	04		with tin/lead solder paste using the standard tin/lead reflow soldering profile. The SnAgCu
Figure 7-48	Void diameter related to land size 1	05		solder ball does not melt; black/grey
Figure 7-49	X-ray image showing uneven heating 1	07		interconnecting fingers are lead-rich grain
Figure 7-50	X-ray image at 45° showing insufficient heating in one corner of the BGA 1	07	,	boundaries; rod shape particles are Ag3Sn IMCs; grey particles are Cu6Sn5 IMCs 120
Figure 7-51	X-ray image of popcorning 1	08	Figure 8-22	Micrograph of a cross-section of a BGA SnAgCu solder ball, assembled onto a board
Figure 7-52	X-ray image showing warpage in a BGA 1	08		with tin/lead solder paste using a backward
Figure 7-53	BGA/assembly shielding examples 1	09		compatibility reflows soldering profile. The SnAgCu solder ball has melted
Figure 8-1	BGA solder joint of eutectic tin/lead solder composition exhibiting lead rich (dark) phase and tin rich (light) phase grains 1	13		Tables
Figure 8-2	Socket BGA solder joints of SnAgCu		Table 3-1	Multichip module definitions
ŭ	composition, showing the solder joint comprised of 6 grains (top photo) and a single grain (bottom photo)	13	Table 3-2	Number of escapes vs. array size on two layers of circuitry
Figure 8-3	Thermal-fatigue crack propagation in eutectic tin/lead solder joints in a CBGA	.0	Table 3-3	Potential plating or component termination material properties
	module 1	14	Table 3-4	Semiconductor cost predictions 1
Figure 8-4	Thermal-fatigue crack propagation in Sn-3.8Ag-0.7Cu joints in a CBGA	4.4	Table 4-1	JEDEC Standard JEP95-1/5 allowable ball diameter variations for FBGA
Figure 0 F	module [3]	14	Table 4-2	Ball diameter sizes for PBGAs 18
Figure 8-5	Incomplete solder joint formation for 1% Ag ball alloy assembled at low end of		Table 4-3	Future ball size diameters for PBGAs 18
	typical process window 1	15	Table 4-4	Land size approximation 18
Figure 8-6	Solder joint failure due to silicon and	4.0	Table 4-5	Future land size approximation 18
F: 0.7	board CTE mismatch		Table 4-6	Land-to-ball calculations for current and
Figure 8-7	Grainy appearing solder joint		Table 4-7	future BGA packages (mm)
Figure 8-8	Nonsolderable land (black pad)		Table 4-7	outlines19
Figure 8-9	Land contamination (solder mask residue) 1			IPC-4101B FR-4 property summaries -
Figure 8-10	Solder ball down			specification sheets projected to better
Figure 8-11	Missing solder ball		Table 4-9	withstand lead-free assembly
Figure 8-12	Deformed solder joint due to BGA warping 1	18	Table 4-9	materials for BGA package substrates
Figure 8-13	Two examples of pad cratering (located at corner of BGA)	18	Table 4-10	Moisture classification level and floor life 30
Figure 8-14	Pad crater under 1.0 mm pitch lead-free solder ball. Crack in metal trace connected		Table 5-1	Environmental properties of common dielectric materials
	to the land is clear; however, the pad crater is difficult to see in bright field microscopy 1		Table 5-2	Key attributes for various board surface finishes
•	Insufficient reflow temperature	19	Table 5-3	Via filling/encroachment to surface finish process evaluation 4-
	insufficient melting of solder joints during reflow soldering. These solder joints are		Table 5-4	Via fill options
Figure 8-16	located below the cam of a socket		Table 6-1	Number of conductors between solder lands for 1.27 mm pitch BGAs
Figure 8-17	Reliability test failure due to very	2 I	Table 6-2	Number of conductors between solder lands
riguic o 17	large void1	21		for 1.0 mm pitch BGAs
Figure 8-18	Comparison of a lead-free (SnAgCu)		Table 6-3	Maximum solder land to pitch relationship 4
	and tin/lead (SnPb) BGA reflow soldering	25	Table 6-4	Escape strategies for full arrays
Eiguro 9 10	profiles	20	Table 6-5	Conductor routing - 1.27 mm Pitch 5-
Figure 8-19	Endoscope photo of a SnAgCu BGA solder ball1	25	Table 6-6	Conductor routing - 1.0 mm Pitch
Figure 8-20	Comparison of reflow soldering profiles for		Table 6-7	Conductor routing - 0.8 mm Pitch
5	tin/lead, backward compatibility and total		Table 6-8	Conductor routing - 1.27 mm Pitch 5-
	lead-free board assemblies 1	26	Table 6-9	Conductor routing - 1.0 mm Pitch 54

March 2008 IPC-7095B

Table 6-10	Conductor routing - 0.8 mm Pitch 54	Table 7-10	Ball-to-void size image - comparison for
Table 6-11	Effects of material type on conduction 66		various ball diameters 104
Table 6-12	Emissivity ratings for certain materials 66	Table 7-11	C=0 sampling plan (sample size for specific index value*)
Table 7-1	Particle size comparisons	Table 7-12	Repair process temperature profiles for tin
Table 7-2	Solder paste volume requirements for		lead assembly 111
	ceramic array packages 73	Table 7-13	Repair process temperature profiles for
Table 7-3	Profile comparison between SnPb and		lead-free assemblies 111
	SAC alloys 75	Table 8-1	Accelerated testing for end use
Table 7-4	Inspection usage application		environments 112
	recommendations 84	Table 8-2	Tin/lead component compatibility with lead-
Table 7-5	Field of view for inspection		free reflow soldering
Table 7-6	Void classification	Table 8-3	Typical stand-off heights for tin/lead balls (in mm)
Table 7-7	Corrective action indicator for lands used with 1.5, 1.27 or 1.0 mm pitch 101	Table 8-4	Common solders, their melting points, advantages and drawbacks
Table 7-8	Corrective action indicator for lands used with 0.8, 0.65 or 0.5 mm pitch 102	Table 8-5	Comparison of lead-free solder alloy compositions in the Sn-Ag-Cu family
Table 7-9	Corrective action indicator for microvia in		selection by various consortia 123
	pad lands used with 0.5, 0.4 or 0.3 mm pitch 103	Table 8-6	Types of lead-free assemblies possible 125

March 2008 IPC-7095B

Design and Assembly Process Implementation for BGAs

1 SCOPE

This document describes the design and assembly challenges for implementing Ball Grid Array (BGA) and Fine Pitch BGA (FBGA) technology. The effect of BGA and FBGA on current technology and component types are addressed, as is the move to lead-free assembly processes. The focus on the information contained herein is on critical inspection, repair, and reliability issues associated with BGAs. Throughout this document the word "BGA" can mean all types and forms of ball/column grid array packages.

- 1.1 Purpose The target audiences for this document are managers, design and process engineers, and operators and technicians who deal with the electronic assembly, inspection, and repair processes. The intent is to provide useful and practical information to those who are using BGAs, those who are considering BGA implementation and companies who are in the process of transition from the standard tin/lead reflow processes to those that use lead-free materials in the assembly of BGA type components.
- 1.2 Intent The new challenge in implementing BGA assembly processes, along with other types of components, is the need to meet the legislative directives that declare certain materials as hazardous to the environment. The requirements to eliminate these materials from electronic components have caused component manufacturers to rethink the materials used for encapsulation, the plating finishes on the components and the metal alloys used in the assembly attachment process.

This document, although not a complete recipe, identifies many of the characteristics that influence the successful implementation of a robust assembly process. In many applications, the variation between assembly methods and materials is reviewed with the intent to highlight significant differences that relate to the quality and reliability of the final product. The accept/reject criteria for BGA assemblies, used in contractual agreements, is established by J-STD-001 and IPC-A-610.

2 APPLICABLE DOCUMENTS

2.1 IPC1

J-STD-001 Requirements for Soldered Electrical and Electronic Assemblies

J-STD-033 Standard for Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices

IPC-T-50 Terms and Definitions for Printed Boards and Printed Board Assemblies

IPC-D-279 Design Guidelines for Reliable Surface Mount Technology Printed Board Assemblies

IPC-D-325 Documentation Requirements for Printed **Boards**

IPC-D-350 Printed Board Description in Digital Form

IPC-D-356 Bare Substrate Electrical Test Information in Digital Form

IPC-SM-785 Guidelines for Accelerated Reliability Testing of Surface Mount Attachments

IPC-2221 Generic Standard on Printed Board Design

IPC-2511 Generic Requirements for Implementation of Product Manufacturing Description Data and Transfer

IPC-2581 Generic Requirements for Printed Board Assembly Products Manufacturing Description Data and Transfer Methodology

IPC-7094 Design and Assembly Process Implementation for Flip Chip and Die Size Components

IPC-7351 Generic Requirements for Surface Mount Design and Land Pattern Standard

IPC-7525 Stencil Design Guidelines

IPC-7711/7721 Rework, Modification and Repair of Electronic Assemblies

IPC-9701 Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments

IPC/JEDEC-9704 Printed Wiring Board Strain Gage Test Guideline

2.2 JEDEC²

JEP95 Section 4.5 Fine Pitch (Square) Ball Grid Array Package (FBGA)

J-STD-020 Handling Requirements for Moisture Sensitive Components

^{1.} www.ipc.org

^{2.} www.jedec.org